Khephren Gould

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Education

University of Victoria — Victoria, BC

Bachelor of Engineering in Electrical Engineering — *Sep. 2022 – Present*

- GPA: 4.32 / 4.33 (8.97 / 9.00 on UVic's 9-point scale)
- Relevant coursework: Computer Systems and Architecture, Design of Digital and VLSI Systems, Real Time Computer Systems Design, Embedded Systems, Digital Signal Processing, Data Analysis and Pattern Recognition
- Awards: Kelly Manning Award - Capstone Design Showcase 1st Place (2026), JCURA Undergraduate Research Award (2026), UVic Tech Challenge Winner (2025), President's Scholarship (2024), Melva J. Hanson Scholarship (2023)

Work Experience

Computer Systems Engineering Co-op — **Elmer's Manufacturing** — Apr. 2025 – Jan. 2026

Altona, MB

- Built a fault-tolerant I^2C memory driver in C with asynchronous read/write, CRC error detection and redundant partitions, giving operators immediate access to actuator controls without blocking on memory
- Implemented a PID control system in C for setpoint control of actuators, replacing an incremental-motion design that users had reported as difficult to operate
- Delivered moisture and temperature sensor integration end to end: Vue.js UI, J1939-compliant CAN communication in Rust, and a Python/SQLite backend, giving farmers grain quality metrics in the field instead of requiring a lab test

Electrical Engineering Co-op — **KJ Controls** — Sep. 2024 – Jan. 2025

Nanaimo, BC

- Produced schematics for Siemens, Motorola and Allen-Bradley PLC and VFD control panels across 20+ projects in mining, forestry and wastewater
- Reviewed datasheets, consultant drawing packages and the Canadian Electrical Code for design compliance; maintained custom AutoCAD Electrical symbol and footprint libraries enabling automatic BOM generation
- Automated datasheet package generation in Python, cutting over 1 hour of engineering time per project

Electrical Engineering Intern — **Laporte** — Jan. 2024 – Apr. 2024

Vancouver, BC

- Drafted electrical design deliverables in AutoCAD including single line diagrams, cable routing layouts and wiring schematics for process improvement projects in agrifood and bioindustrial plants
- Maintained load calculation and wire sizing spreadsheets used to develop panel schedules and size overcurrent protective devices

Projects

Anduril 3 Sensor and Data Acquisition System | *KiCad, STM32, C, FreeRTOS, CAN*

- Designed 9 distributed data acquisition nodes reporting to a flight computer over a 1 MHz CAN bus, reading 12 three-gauge strain rosettes, 4 SPI pressure ports and 4 platinum RTDs
- Designed a 4-layer mixed-signal PCB with bridge completion, anti-alias filtering, a 24-bit ADC and an STM32G4; optimised the signal chain to \$4.50 per input, with simulated integrated noise of 72 μVrms and simulated gain error of 0.92%
- Recovered strain data from 7 of 9 gauges and 3 of 4 temperature sensors in flight

FPGA-based 16-Bit Pipelined CPU | *VHDL, Xilinx Vivado, Computer Architecture*

- Implemented a 5-stage pipelined Harvard architecture processor supporting a full load/store ISA, extended with a branch-on-overflow instruction backed by a dedicated status flag
- Resolved data hazards with an operand forwarding unit and load-use stall detection, giving a 20% speedup over stalling; 1653 LUTs, 532 registers, verified on hardware

Fixed-Point Digital Filters for the ARM Cortex-A7 | *C, ARM NEON, Fixed-Point DSP*

- Optimised a 4th order Butterworth IIR filter from a soft floating-point reference: software pipelining reached 27.2x and NEON SIMD 33.5x by raising ILP and eliminating register spilling
- Diagnosed limit cycles caused by a 112.4 dB coefficient dynamic range overrunning a 32-bit accumulator; restructured as cascaded biquads with saturating arithmetic

Early Stage Wildfire Detection System | *STM32U5, LoRa, C, LTspice*

- Built a wireless sensor network to make early wildfire detection affordable in high-risk areas: solar-powered nodes pairing an STM32U5 with an SX1262 LoRa transmitter and a BQ25570 energy harvesting stack, reporting to an ESP32-based gateway
- Owned the embedded software. Cut MCU power consumption a further 10.2% with a timer-interrupt sleep and wake scheme, verified on a Nordic power profiler, and modelled the harvester in LTspice at 16 days of battery-backed operation
- Measured reliable LoRa communication at 300 m through obstruction; link budget projects 1 km at a 30 dB forest fade margin

Skills

Languages: C (FreeRTOS, STM32 HAL), C++ (SFML), Rust (tokio), VHDL, Python (FastAPI, Selenium, NumPy, SciPy), SQL (SQLite), MATLAB, ARM assembly (NEON), MIPS assembly

Hardware: PCB design (KiCad), Xilinx Artix-7 (Basys 3, Nexys A7), Zynq UltraScale+ MPSoC (Kria), AMD MicroBlaze, STM32 (G4, U5, F4), NXP K32, ATmega328, ESP32, ARM Cortex-A7, RTL-SDR

Protocols: CAN / J1939, SPI, I^2C, UART, AXI, LoRa

Tools: Linux (Git, Make, GCC, grep), Bitbucket, ClickUp, Docker, Redis, Vivado, STM32CubeIDE / MX, PlatformIO, LTspice, AutoCAD Electrical, Onshape