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Strain Gauge Signal Conditioning System

ENGR 446 Final Report

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University of Victoria
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Monty Raisinghani, Instructor
ENGR 446, Summer 2026
Department of Engineering
University of Victoria

Re: ENGR 446 Report on the Strain Gauge Signal Conditioning System

Dear Mr. Raisinghani,

This report, titled "Strain Gauge Signal Conditioning System," is submitted for the ENGR 446 Technical Report. The author is an electrical engineering student studying in term 4B of his undergraduate degree at the University of Victoria. The purpose of this report is to conduct design, analysis and provide recommendations for a realizable low-cost strain gauge signal conditioning system. The goal is to provide student design teams and academics interested in conducting strain analysis with a reference design that can be implemented cheaply.

The scope of this report covers the design and evaluation of the amplifier and filter stages for a signal conditioning system for bonded metallic strain gauges. The excitation circuit is assumed to be a quarter bridge and an industry standard ADC (AD4170-4) was used to benchmark the signal conditioning circuits. Vibration analysis on a cantilever beam experiencing blunt force impact was used as a model problem through the use of open source strain data provided by the DROPBEAR project [1]. Active and passive second order lowpass configurations were considered for the filter stage while both differential and instrumentation amplifiers were considered for the amplifier stage. Analysis was conducted using Analog Devices Signal Chain Designer resulting in quantifiable error, noise, and cost metrics that were used to perform a comparative analysis.

The report recommends a configuration consisting of a 2nd order lowpass RC filter paired with the AD8429 instrumentation amplifier. This design provided the best noise performance and the lowest gain error of the four candidates (16.5 µVrms total integrated noise referred to the ADC input, 0.694% relative error, 73.3 mV offset error) while retaining a cost of $40.93 per input.

The author would like acknowledge the members of the High-rate Structural Monitoring, Damage Detection, Prognostics, and Reactions Working Group of Iowa State University for producing the dataset used as a basis for design in this report.
Regards,

Khephren Gould
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Contents

List of Figures

List of Tables

Executive Summary

The bonded metallic strain gauge is the most commonly used strain measurement device. This report presents a reference design for a low-cost signal conditioning system for bonded metallic strain gauges. The goal is to provide student design teams and academics interested in conducting strain analysis with a reference design that can be implemented cheaply.

To ensure practical applicability, design constraints for required bandwidth, and input signal range were based on open source strain gauge data provided by the High-rate Structural Monitoring, Damage Detection, Prognostics, and Reactions Working Group of Iowa State University. The report investigated 4 preliminary design options created by pairing two filter options (2nd order passive RC lowpass, active Sallen-Key) with two amplifier options (differential, instrumentation). Analog Devices Signal Chain Analyzer was used for schematic capture and simulation of the circuits. Noise and error simulation was performed resulting in quantifiable metrics for total integrated noise, total offset error and total gain error. These parameters along with costs of the simulated components were used in a comparative analysis.

The analysis concluded that the 2nd order passive RC filter combined with the insturmentation amplifier yielded a total integrated noise of 16.5 µVrms referred to the ADC input, total offset error of 73.3 mV and total gain error of 0.694%. The resulting circuit theoretically allows a resolution of +/- 0.024$\mu\epsilon$ with relative error below 34 µϵ at +/- 4mV full scale and supports sampling frequencies up to the 25kHz required by the open source dataset. The cost of the final system was estimated at $40.93 per input which is a fraction of the cost of alternative commercial solutions.

The results of this report can be used to reduce the costs of performing strain measurement, and provide a cost estimate for groups investigating strain instrumentation while being completely independent of the size and form factor of the final signal conditioning device. In further investigations it is recommended to consider alternative excitation sources for the sensor (constant current, AC carrier wave). A complete system also requires careful design of the power supply as well as mixed signal PCB layout which was deemed outside the scope of this report.

Glossary and List of Symbols

Glossary

AC Alternating current.

ADC Analog-to-digital converter.

Bonded metallic strain gauge A strain gauge consisting of a metallic foil or wire grid bonded to the surface of a test specimen.

Butterworth response A filter response with a maximally flat passband.

CMRR Common-mode rejection ratio. The ability of a differential or instrumentation amplifier to reject the common-mode component of its two inputs.

DC Direct current.

Diff Differential amplifier, used as shorthand in the candidate design names.

Differential amplifier A single op-amp circuit that amplifies the difference between two input voltages.

Drift Change in the gain or offset of a component caused by a change in temperature.

DROPBEAR Dynamic Reproduction of Projectiles in Ballistic Environments for Advanced Research. The open source cantilever beam strain dataset used as the model problem for this report.

Effective resolution The number of bits of ADC output that carry signal rather than noise.

Excitation voltage The DC voltage applied across the Wheatstone bridge.

Full scale The largest input span the signal chain is designed to accept.

Gain error An error proportional to the input signal, expressed as a percentage or in ppm.

Gauge factor Ratio relating fractional resistance change to strain.

In Instrumentation amplifier, used as shorthand in the candidate design names.

INL Integral nonlinearity. The deviation of an ADC transfer function from a straight line after zero and gain errors are removed.

Instrumentation amplifier A three op-amp differential amplifier with high input impedance and high CMRR, available as a single integrated circuit.

Johnson noise Thermal noise generated by a resistance, also called thermal or Nyquist noise.

Microstrain A strain of 10^{-6} m/m.

Nyquist sampling theorem The result that a sampled signal is bandlimited to half the sampling rate.

Offset error An error independent of the input signal, expressed as a voltage.

Op-amp Operational amplifier.

PCB Printed circuit board.

ppb Parts per billion.

ppm Parts per million.

Quarter bridge A Wheatstone bridge in which one of the four arms is an active strain gauge and the remaining three are fixed completion resistors.

rms Root mean square.

RSS Root sum square. A method of combining independent error sources as the square root of the sum of their squares.

RTA Referred to the ADC input. A noise or error quantity expressed at the input of the converter, after the amplifier gain has been applied.

Sallen-Key filter An active second order filter topology using a single op-amp.

Signal Chain Analyzer The Analog Devices schematic capture and simulation tool used for the noise and error analysis in this report.

SK Sallen-Key filter, used as shorthand in the candidate design names.

Two-point calibration A correction procedure that removes offset and gain error by measuring two known input values.

Wheatstone bridge A four-arm resistive bridge that converts a resistance change into a differential voltage.

Worst case error analysis A method of combining error sources by adding their magnitudes linearly.

Zero error The ADC offset error, measured at zero differential input.

List of Symbols

A Cross-sectional area of the gauge conductor (m^2).

A_v Filter passband gain (dimensionless).

BW Noise bandwidth (Hz).

BW_{in} Input signal bandwidth (Hz).

C Capacitance (F).

e_n Voltage noise density ($nV/\sqrt{Hz}$).

f_c Filter cutoff frequency (Hz).

f_s ADC sampling rate (Hz).

G Gain (dimensionless) / gauge factor, per context.

$H(\omega)$ Filter frequency response (dimensionless).

i_n Current noise density ($pA/\sqrt{Hz}$).

k Boltzmann constant (J/K).

L Conductor length (m).

N_{eff} Effective resolution (bits).

Q Filter quality factor (dimensionless).

R Resistance (Ω).

ΔR Change in gauge resistance (Ω).

R_G Instrumentation amplifier gain setting resistor (Ω).

R_{in} Input impedance of an amplifier stage (Ω).

R_s Source impedance presented by the bridge (Ω).

$S(\omega)$ Noise power spectral density (V^2/Hz).

T Absolute temperature (K).

V_{in} Full-scale bridge output span (V).

V_o Output voltage (V).

V_{range} Portion of the ADC input range occupied by the signal (V).

V_{ref} ADC reference voltage (V).

V_s Excitation (source) voltage (V).

V_{shift} Level shift voltage applied to the amplifier (V).

V_{sig} Amplified signal span at the ADC input (V).

$v_{n,rms}$ Total rms noise at the ADC input (V).

$\overline{v_n^2}$ Total mean-square noise voltage (V^2).

ε Mechanical strain ($\mu\varepsilon = \mu$m/m).

ρ Resistivity of the gauge conductor (Ω·m).

ω Angular frequency (rad/s).

ω_c Filter cutoff (natural) frequency (rad/s).

1 Introduction

Strain gauges are widely used to measure deformation, force, pressure, torque, and structural loading. They are used heavily in civil engineering for structural monitoring of cable bridges or building support structures. Aerospace and automotive manufacturers use them to monitor loading on key components. They also have applications for flow rate monitoring in medical instruments [2].

1.1 Theory - Strain Gauges

The bonded wire strain gauge is the most commonly employed strain measurement solution. An image of such an instrument is shown in Figure 1 from Hoffman [3].

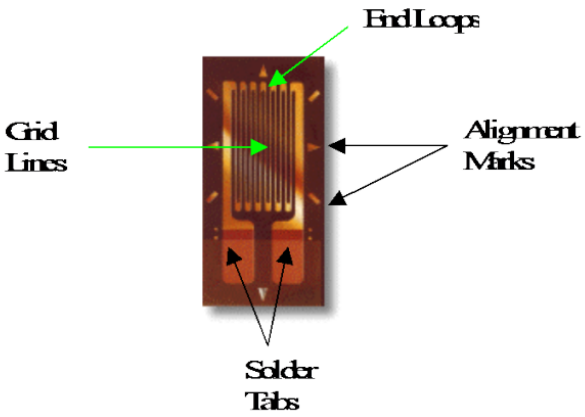

Figure 1: Bonded Wire Strain Gauge

The strain gauge operates by changing its resistance in response to deformation (strain). The change in resistance results from the deformation's effect on the ratio of the length to the cross sectional area of the conductive grid lines on the gauge (reflected by equation 1)

$$R = \frac{\rho L}{A} \tag{1}$$

where R is the gauge resistance (Ω), ρ is the resistivity of the grid material (Ω·m), L is the conductor length (m), and A is the cross-sectional area (m^2). When rewritten in terms of a resistance-strain relationship, the defining equation for the strain gauge results (equation 2).

$$G\varepsilon = \frac{\Delta R}{R} \tag{2}$$

G is the gauge factor, a dimensionless datasheet parameter denoting the sensitivity of the device to deformation, and ϵ is the strain in $\frac{m}{m}$.

1.2 Theory - Signal Conditioning

Many strain gauge applications require remote and autonomous data acquisition. For applications such as road or in-flight testing it is not feasible for an engineer or technician to manually record observations of a measurement device. For these applications data must be digitized and stored for post processing after the test. An analog to digital converter is typically employed for this purpose. Due to the milliohm output range of typical bonded wire gauge configurations, signal conditioning is required before the gauge is connected to the ADC. Without signal conditioning, even high performance 24-bit ADC's introduce sufficient quantization noise to render the strain measurements useless. Note that an ADC measures voltage and in equation 2 the lack of a voltage parameter. The Wheatstone Bridge circuit invented by Sir Charles Wheatstone in 1833 is almost always employed for converting the change in resistance of the gauge (ΔR) to a voltage that can be sampled and stored. When wired in a quarter bridge configuration, bridge voltage is related to ΔR by equation 3.

$$V_o = \frac{V_s}{4} \cdot \frac{\Delta R}{R} \tag{3}$$

where V_o is the bridge output voltage (V), V_s is the excitation voltage (V), ΔR is the resistance change of the active gauge (Ω), and R is the nominal gauge resistance (Ω). It is this voltage that is filtered and amplified by the signal conditioning circuit. Typically, the stage following the bridge is the amplifier.

Amplifier design is discussed in Horrowitz and Hill chapter 5 [4]. The equation below is the effective resolution of an ADC in bits which dictates the smallest change in input that can be meaningfully detected.

$$N_{eff} = \log_2\left(\frac{V_{range}}{v_{n,rms}}\right) = \log_2\left(\frac{GV_{in}}{v_{n,rms}}\right) \tag{4}$$

where N_{eff} is the effective resolution (bits), V_{range} is the portion of the converter's input range occupied by the signal (V), equal to the amplified signal span GV_{in}, G is the amplifier gain, V_{in} is the full-scale bridge output span (V), and $v_{n,rms}$ is the total rms noise at the converter input (V). The amplifier stage manages a trade between two noise sources on opposite sides of the converter. On the digital side, the ADC contributes a fixed noise floor consisting of its quantization step and internal noise. On the analog side, every element ahead of the converter (the bridge, the amplifier itself, the filter) contributes noise that is *amplified along with the signal*.

Gain shifts the balance between them and is typically selected such that GV_{in} is maximally close to the maximum input range allowed by the ADC. The next stage, the filter, is beneficial for reducing the impact of the amplified noise.

As discussed in Zumbahlen, Analog Filters, the value of low-pass filtering is best understood in the frequency domain [5]. Noise contributions by the bridge circuit, amplification circuit, and surrounding environment are modeled not as a single tone but a continuum of frequency components, each contributing a small, randomly-timed oscillation. The magnitude of the oscillation is described by the noise spectral density $S(\omega)$, and the total noise reaching the ADC is the area under this density across every frequency the filter passes:

$$\overline{v_n^2} = \frac{1}{2\pi} \int_{-\infty}^{\infty} S(\omega) \, |H(\omega)|^2 \, d\omega \tag{5}$$

where $\overline{v_n^2}$ is the total mean-square noise voltage at the filter output (V^2), $S(\omega)$ is the noise power spectral density (the mean-square noise voltage per unit bandwidth in V^2/Hz at each frequency), and $H(\omega)$ is the filter's frequency response [5]. Because the noise components are random and independent, they occasionally drift into alignment; the more of them the filter passes, the larger these chance alignments become, appearing as noise spikes in the measured waveform. Total noise thus grows with filter bandwidth. A well-designed low-pass filter counters this. By driving $|H(\omega)|$ toward zero beyond the cutoff ω_c the integral is effectively taken over a smaller range of frequencies, shrinking the mean noise voltage. Since the strain signal occupies only a narrow low-frequency band, the filter discards noise while leaving the measurement untouched.

1.3 Theory - Noise and Error in Analog Circuits

The ideal signal conditioning circuit would provide infinite resolution and have no measurement error. In practice, the resolution of a signal conditioning system is limited by the noise introduced by the circuit elements present in the system. This report focuses on noise effects introduced by op-amps and resistors. As discussed in greater depth below, this report used Analog Devices Signal Chain Analyzer to perform error and noise simulations.

1.3.1 Noise

Random noise is characterized by its density and has units $nV/\sqrt{Hz}$. An op-amp (and differenial / instrumentation amplifiers by extension) have noise performance described by two parameters:

1. Voltage Noise Density (e_n)
2. Noise current (i_n)

Noise current can be converted to an equivalent noise voltage by multiplying by the source resistance of the signal. Although more complex sources of noise such as flicker, and shot noise are present in real circuits, they are not considered in this report. If a noise source is uniform over frequency ("white noise") the total integrated noise (from equation 5) is $v_n = e_n\sqrt{BW_{in}}$. Another source of noise is Johnson noise generated by resistive elements in the circuit. Johnson noise results from random thermal fluctuations within the resistor and is uniformly distributed like the voltage and current noise of amplifiers. It is described by the equation $v_{noise}(rms) = (4kTRBW)^{1/2}V(rms)$ where T is the absolute temperature in Kelvin, BW is the signal bandwidth in hertz, R is the resistance and k is the Boltzman constant. As discussed above, a filter attenuates a portion of the frequencies present in the input signal and the resulting noise voltage at the output of the filter is obtained by computing the integral in equation 5. The final source of noise considered is ADC rms noise. The rms noise is an empirical datasheet parameter that is obtained through experimental testing of the final device. As quantization noise is a component, choosing an ADC with

more output bits will reduce this quantity. All designs in this report use the AD4170-4, a 24 bit ADC capable of 500kHz sampling. Appendix C contains an excerpt from the datasheet which details the methodology through which rms noise for this ADC is determined.

The Signal Chain Analyzer software determines the bandwidth (BW) over which the integral should be computed using the sampling rate of the ADC. The Nyquist Sampling Theorem guarantees that the bandwidth of the digitized signal is limited to half the sampling rate. Thus, Signal Chain Analyzer computes the integral up to half the sampling rate of the ADC used in the simulation [6].

1.3.2 Error

Error in signal conditioning is introduced by the operational amplifiers present in the system. The 4 sources of error introduced by the signal conditioning system amplifiers are:

1. Offset voltage
2. Input offset and bias current
3. Gain error
4. CMRR related error

The CMRR is a parameter for differential and instrumentation amplifiers that dictates how well the amplifier rejects the common mode DC bias of the differential inputs. For the wheatstone bridge excited at 3.3V this common mode is 1.65V while the actual signal (which appears on top of the DC bias) is only +/- 4mV. Amplifiers with poor CMRR introduce an offset error [4].

The passive components introduce error due their tolerance. The tolerance of the resistors is included in the error analysis as a gain error (resistors set the gain of the amplifier). Finally, the ADC introduces three terms to the error:

1. Zero Error
2. Gain Error
3. Integral Nonlinearity error

Note that all the components above also have drift error; changes in gain and offset due to change in temperature. This report does not consider these errors. All error simulations were performed at a single temperature of 25^oC. For the purposes of this report, total error is obtained by combining the error sources by adding them linearly. This is referred to in the literature as worst case error analysis. The statistical theory of error analysis indicates that RSS (root sum square) error combination is the most accurate however it is omitted to simplify the analysis [4].

1.4 Objective and Problem Definition

The purpose of this project is to design a strain gauge signal conditioning system that achieves accuracy comparable to commercial solutions at lower cost. The design targets: (1) amplification to the full-scale range of 0–3.3 V with the AD4170-4 ADC used as a common benchmark between all designs; (2) conditioning a gauge with ±4 mV full-scale output and 350 Ω nominal resistance; and (3) maintaining amplification across the full signal bandwidth.

1.5 Scope and Limitations

This report considers a comparative analysis of only the signal conditioning stage. Noise and error analysis encompasses the entire signal chain (including the sensor and ADC) however the sensor and ADC are held constant throughout the analysis to allow the performance of only the signal conditioning circuit to be isolated. The sensor is a quarter bridge with 350Ω nominal resistance and the ADC is assumed to be the AD4170-4, a 24-bit ADC that supports sampling up to 500kHz. The design is limited to op-amp-level analysis; transistor-level design, external error sources (gauge non-linearity, lead-wire resistance, supply noise), and filter orders above second are excluded. Additionally, assumptions must be made about the power supply. A power supply capable of +/-5V output is assumed. It is assumed that the ADC reference voltage and the wheatstone bridge are powered through a 3.3V regulator. Finally, assumptions must be made about the tolerances of the passive components used. These are used in the calculation of parameters such as Johnson noise of a resistor. It is assumed that the bridge completion resistors are high precision 350Ω with 0.05% tolerance. All other components are assumed to have a 0.5% tolerance.

1.6 Methodology

As described previously, the goal of this report is to propose a low cost design for the amplification and filter stages of a signal conditioning system. The design target is a system with sufficient gain and bandwidth to meet the requirements of the DROPBEAR dataset model problem, which involves strain measurements on a vibrating cantilever beam.

Data from test setup 2, trial 12 was used as a sample input. The plot of bridge output vs time allows the input voltage range and signal bandwidth to be determined by inspection. The nominal gauge resistance and sampling rate were obtained from the project's Github repository [1]. Table 1 summarizes the model problem parameters used as constraints for signal conditioning system design.

Table 1: Engineering Analysis Inputs

Parameter	Symbol	Value
Input Signal Amplitude	V_{in}	4 mV
Input Signal Bandwidth	BW_{in}	160 Hz
ADC Sampling Rate	f_s	25.6 kHz
ADC Reference Voltage	V_{ref}	3.3 V
Input Signal Source Impedance	R_s	350 Ω

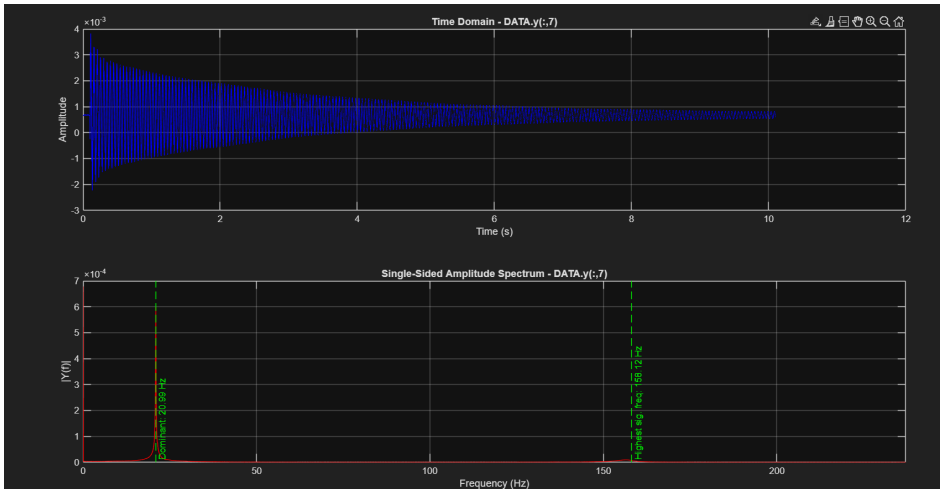

Figure 2: Model Strain Gauge Input

Four solutions are proposed. Instrumentation amplifier and differential amplifier circuits were designed following the methodology in Horrowitz and Hill Chapter 5 [4]. 2nd order RC Low pass and Sallen-Key filters were designed following the method proposed in Su, Analog Filters [7]. Design calculations are presented in Appendix A. The 4 solutions proposed consist of all possible combinations of the filter and amplfier circuits considered.

The four solution candidates are evaluated on the basis of error performance, noise performance, and cost. The sample error budget from chapter 5 section 1 of Horrowitz and Hill is used to determine the error performance and is populated with the output of error simulation performed by Analog Devices Signal Chain Analyzer. A noise budget is also obtained from Signal Chain Analyzer using the noise simulation feature. The four candidate signal conditioning solutions were compared using the weighted objectives matrix in Table 2, which evaluates each design for noise performance, error performance, and cost.

Table 2: Weighted objectives matrix.

Criterion	**Weight (%)**	**Diff+RC**	**In+RC**	**Diff+SK**	**In+SK**
Noise performance	50				
Cost	30				
Offset Error performance	10				
Gain Error performance	10				
Total					

All noise and error totals reported in this document are referred to the ADC input (RTA): they are quoted at the point where the signal conditioning chain meets the converter, after the amplifier gain has been applied. Referring to the ADC input compares the four candidates on the quantity that limits the digitized measurement, and makes every total directly comparable to the converter's 3.3 V full-scale range.

To give the scoring bands physical meaning, RTA voltages are also expressed as an equivalent strain. For a quarter bridge with gauge factor $G = 2$ excited at $V_s = 3.3\,\mathrm{V}$, the

bridge sensitivity is $V_o/\varepsilon = V_s G/4 = 1.65\,\mu\text{V}/\mu\varepsilon$. With the signal conditioning gain of 412 required to map the $\pm 4\,\text{mV}$ bridge output onto the converter's 3.3 V range, one microstrain corresponds to 0.681 mV at the ADC input, and full scale corresponds to $\pm 2424\,\mu\varepsilon$ (a span of $4848\,\mu\varepsilon$).

Table 3: Noise performance evaluation

Total Integrated Noise, RTA (μV rms)	**Equivalent ($\mu\varepsilon$ rms)**	**Numerical Score**
> 160	> 0.24	0
80–160	0.12–0.24	2
40–80	0.06–0.12	4
20–40	0.03–0.06	6
10–20	0.015–0.03	8
< 10	< 0.015	10

Table 4: Offset error evaluation

Total Offset Error, RTA	**Equivalent ($\mu\varepsilon$)**	**Numerical Score**
$> 250\,\text{mV}$	> 367	0
200–250 mV	294–367	2
150–200 mV	220–294	4
100–150 mV	147–220	6
50–100 mV	73–147	8
$< 50\,\text{mV}$	< 73	10

Table 5: Gain error evaluation

Total Relative Error (%)	**Equivalent ($\mu\varepsilon$)**	**Numerical Score**
> 1.50	> 73	0
1.10–1.50	53–73	2
1.00–1.10	48–53	4
0.75–1.00	36–48	6
0.55–0.75	27–36	8
< 0.55	< 27	10

Noise Performance was assigned the highest weight (50%) because it directly limits the smallest change in strain that can be measured. Unlike offset voltage and gain error, which can be calibrated if desired, random noise cannot be removed after the fact and directly sets the smallest change in strain that can be detected by the system. The noise bands in Table 3 are spaced by octaves, so each two-point step in the score corresponds to a factor of two in total integrated noise, which by equation 4 is one additional bit of effective resolution. Across the 3.3 V converter range the bands span 14.3 to 18.3 effective bits.

Cost was weighted second-highest (30%), because the project has the goal of achieving commercial-comparable accuracy at lower cost. The cost will be evaluated by comparing the relative cost of each solution. The lowest cost solution will be given a ranking of 10 and the highest cost solution a ranking of 2.

The cost evaluation was conducted to provide a realistic estimate of what a full data acquisition system built around each signal conditioning circuit would cost, rather than a comparison of the signal conditioning components alone. A comparison restricted to the amplifier and filter components would exaggerate the relative difference between the four candidates, because those components account for only part of the cost of a working instrument. Reporting the figure at the system level instead expresses the difference between candidates as a fraction of the total expenditure a design team faces, which is the relevant quantity given the goal of reducing the cost of strain measurement.

Each cost budget includes the supporting hardware required to turn the signal conditioning circuit into a usable acquisition channel: the bridge completion resistors, the AD4170-4 ADC used as a benchmark across all four designs, an STM32F0 microcontroller to manage the converter and transfer the digitized data, the power distribution components, and the cost of PCB manufacturing and assembly. The amplifier, filter, and gain setting components are the only items that differ between candidates. Every other line item is held constant, so the difference between the reported totals is attributable to the choice of signal conditioning topology alone.

Several of these items are shared across channels rather than duplicated per input. A single AD4170-4 provides four differential inputs, and the microcontroller, power distribution, and PCB are shared by the whole instrument. An eight-channel instrument is assumed as the reference configuration, so the cost of each shared item is divided by eight and amortized across the channels it serves. This is indicated in the cost tables by a ($\div 8$) annotation on the affected line items. All totals are reported on a per-channel basis, which allows the cost of a system to be estimated by multiplying by the required channel count.

Offset and relative error were weighted lower (10%) because these errors can largely be removed through a two-point calibration procedure. Once calibrated, offset and gain errors are corrected, leaving only the components the integral non-linearity (INL).

The offset bands in Table 4 are spaced in uniform 50 mV increments, each step representing approximately 1.5% of the converter's full-scale range or 73 $\mu\varepsilon$ referred to the gauge. Uniform spacing is appropriate here because offset is a systematic error that adds linearly to the measurement, so equal increments of offset represent equal increments of uncorrected measurement error. Any total below 50 mV scores full marks, because a residual of that size is recoverable by the two-point calibration described above. The lowest band is placed at 250 mV, beyond which the offset exceeds the worst-case contribution of every other error term combined.

The gain error bands in Table 5 are anchored to the passive tolerance floor. A 0.5% gain resistor sets a floor near 0.5% where a single resistor sets the gain, and near 1.0% where two tolerances combine linearly under the worst-case summing assumption stated above, so 0.55% and 1.10% are used as band edges. Relative error is dimensionless and is therefore unchanged by referring the budget to the ADC input.

2 Discussion

2.1 Candidate Solutions

Four candidate solutions are formed by combining two amplifier topologies (instrumentation, differential) with two filter topologies (passive RC, Sallen-Key active).

2.1.1 Comparison of Differential and Instrumentation Amplifier Topologies

As discussed in Horrowitz and Hill, both differential and instrumentation amplifiers are commonly used in precision analog design.

The differential amplifier circuit is shown in Figure 3.

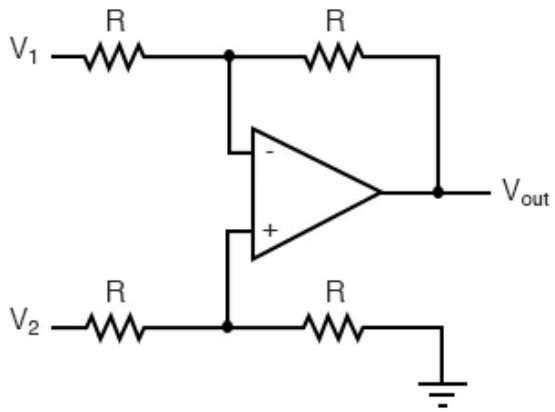

Figure 3: Differential Amplifier Circuit

The amplifier gain is set by equation 6

$$v_o = \frac{R_2(1+\frac{R_1}{R_2})}{R_1(1+\frac{R_3}{R_4})}v_2 - \frac{R_2}{R_1}v_1 \tag{6}$$

Setting $\frac{R_3}{R_4} = \frac{R_1}{R_2}$ we can write the relationship as $v_o = G(v_2 - v_1)$ with $G = \frac{R_2}{R_1}$ which is a gain applied to a differential signal as desired.

The instrumentation amplifier circuit is shown in Figure 4

The gain of the instrumentation amplifier is determined by equation 7. Note that modern packages combine all three op-amps in a single integrated circuit that allows gain setting through R_g.

$$1 + \frac{2R}{R_G} \tag{7}$$

The main tradeoffs between the two amplifiers are in the cost, CMRR and input impedance. Typically, instrumentation amplifiers have a higher cost but also a higher CMRR compared to differential amplifiers [4]. The instrumentation amplifier also has a much higher input

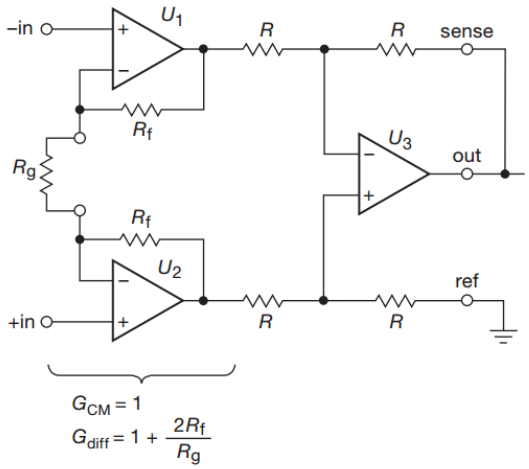

Figure 4: Instrumentation Amplifier Circuit

impedance than the differential amplifier. This allows the use of smaller gain setting resistors which can reduce the impact of Johnson noise. The design of both the differential and instrumentation amplifier circuits is presented in appendix A. The AD8429 was selected for use as an instrumentation amplifier while the ADA4098-2 was selected as an op-amp for the differential amplifier circuit.

2.1.2 Comparison of Passive and Active 2nd Order Analog Filters

Su discusses the design of both passive and active second order filters. The circuit schematic for a 2nd order RC filter is shown in Figure 5.

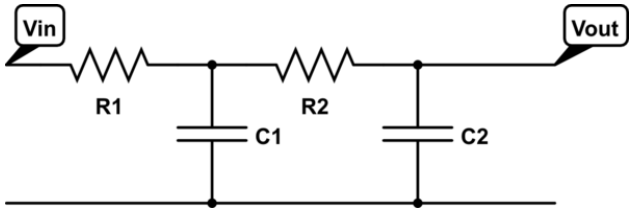

Figure 5: 2nd Order RC Filter Schematic

The frequency response of the first order RC filter is presented as shown in equation 8.

$$H(\omega) = \frac{1}{1 + j\omega RC} \tag{8}$$

The design methodology presented in Chapter 9 of Su is performed in appendix A [7].

The active 2nd order filter considered is the Sallen-Key Filter. The schematic for this filter is shown in Figure 6

The frequency response of the Sallen-Key Filter is shown in equation 9.

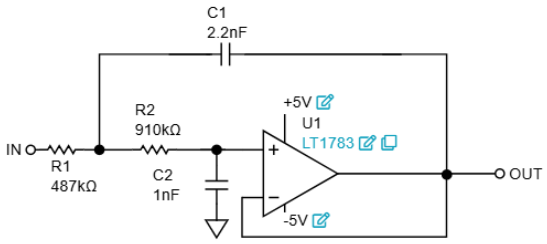

Figure 6: Sallen-Key Filter Circuit

$$H(s) = \frac{A_v\,\omega_c^2}{s^2 + \dfrac{\omega_c}{Q}\,s + \omega_c^2} \tag{9}$$

where A_v is the amplifier passband gain, ω_c is the cutoff (natural) frequency (rad/s), and Q is the quality factor (dimensionless). As with the second order passive RC, Su presents a design methodology for this filter which is performed in appendix A.

Although the Sallen-Key can improve some non idealities with a passive, cascaded 2nd order filter (loading between stages, distortion in the filter passband) the use of an op-amp adds noise and cost to the circuit.

2.2 Simulation

After performing the circuit designs, the circuits were implemented in Signal Chain Analyzer. The noise and error totals presented below are the aggregate of the individual stage contributions; the per-stage Signal Chain Analyzer outputs from which they are assembled are reproduced in Appendix B.

The final schematic for the differential amplifier and 2nd order RC filter is shown in Figure 7.

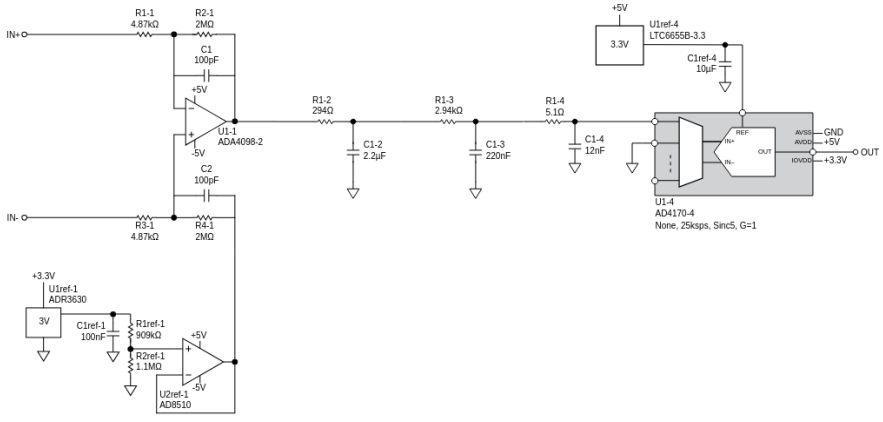

Figure 7: Differential Amplifier and RC Filter Circuit

Note in the circuit, the inclusion of the ADC and power supply components which remain constant throughout all four of the signal conditioning designs. The Signal Chain Analyzer noise report is shown in Figure 8. Observe that the amplifier contributes significant noise to

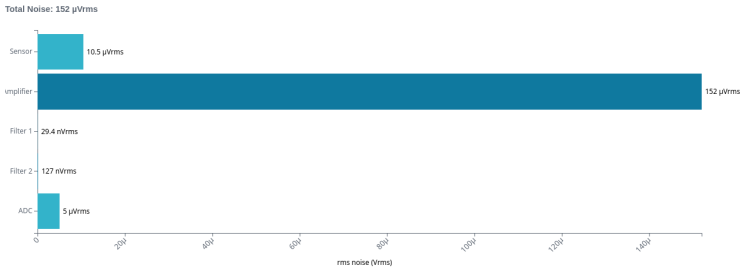

Figure 8: Diff Amp + RC Noise Totals

the total integrated noise of 152 μVrms referred to the ADC input. This is due to Johnson noise in the large gain setting resistor which is required to ensure the input impedance of the amplifier dominates the output impedance of the source. The error budget for the design is presented in Table 6

Table 6: Error Budget: Diff Amp + RC

Category	**Offset Error**	**Rel. Error**
Total		
Total Error	56.1mV	1.03%
ADC		
Zero Error	80 μV	–
Gain Error	–	250 ppm
INL	–	2.5 ppm
Op Amp		
Offset Voltage	13.9 mV	–
Offset Current	1.4 mV	–
CMRR	–	499 ppb
Resistors		
R1 Tol.	19.9 μV	6.12 ppm
R2 Tol.	20.1 μV	0.499%
R3 Tol.	19.7 μV	0.477%
R4 Tol.	19.9 μV	6.23 ppm
Filter		
Filter R1 Tol.	–	–
Filter R2 Tol.	–	–

In this case, the filter resistors do not contribute to error because the DC gain of the filter is independent of the resistor value. The costs of the resulting signal conditioner are presented in table 7.

Table 7: Costs: Diff Amp + RC

Component	**Qty**	**Unit $**	**Total $**
ADA4098-2 Amplifier	1	9.33	9.33
0.5% Resistors	6	0.10	0.60
0.5% Capacitors	2	0.10	0.20
0.05% Resistors (bridge)	4	4.20	16.80
AD4170-4 ADC (÷8)	1/8	29.33	3.67
STM32F0 (÷8)	1	0.31	0.31
Power Distribution (÷8)	1/8	4.10	0.51
PCB Manufacturing and Assembly (÷8)	1/8	10.00	1.25
Total (per channel)			**32.66**

The circuit for the differential amplifier and Sallen-Key filter is shown in Figure 9

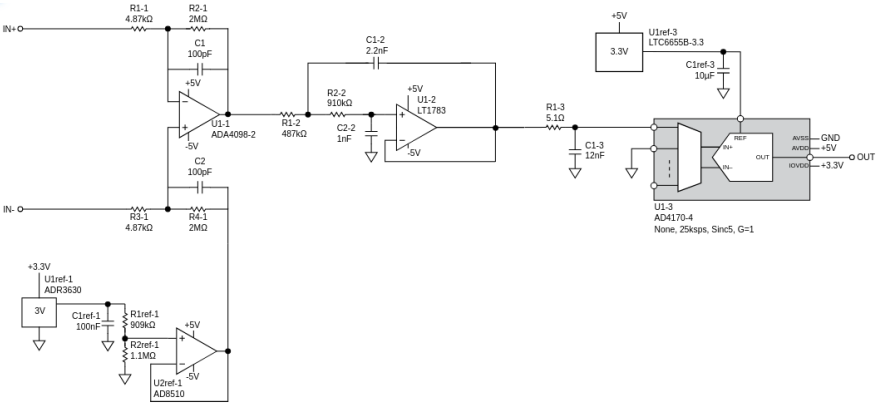

Figure 9: Diff Amp + Sallen-Key Circuit

A noise simulation was performed and the results are presented in Figure 10. The noise

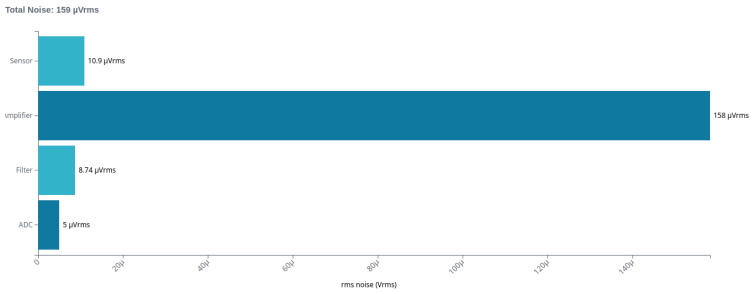

Figure 10: Diff Amp + Sallen-Key Noise Totals

performance indicates the same issue with the design as in the 2nd order passive RC case. The noise total is dominated by the amplifier stage due to resistor Johnson noise. The addition of the op-amp in the filter stage slightly worsens noise performance, raising the total integrated noise to 158 μVrms referred to the ADC input from the 152 μVrms of the passive RC design. Error calculations were also performed and are summarized in Table 8.

Table 8: Error Budget: Diff Amp + SK

Category	**Offset Error**	**Rel. Error**
Total		
Total Error	168mV	1.03%
ADC		
Zero Error	80 μV	–
Gain Error	–	250 ppm
INL	–	2.5 ppm
Op Amp		
Offset Voltage	13.9mV	–
Offset Current	1.4mV	–
CMRR	–	499 ppb
Resistors		
R1 Tol.	19.9 μV	6.08 ppm
R2 Tol.	20.7 μV	0.499%
R3 Tol.	19.8 μV	0.477%
R4 Tol.	20.5 μV	6.23 ppm
Filter Op Amp		
Offset	800 μV	–
Bias Current	112 mV	–
Offset Current	12.2 pV	–
CMRR	–	31.6 ppm
Filter Resistors		
R1 Tolerance	–	–
R2 Tolerance	–	–

Finally, the costs of this circuit were determined and are presented in Table 9.

Table 9: Costs: Diff Amp + SK

Component	**Qty**	**Unit $**	**Total $**
ADA4098-2 Amplifier	1	9.33	9.33
LT1783 Amplifier	1	5.56	5.56
0.5% Resistors	6	0.10	0.60
0.5% Capacitors	2	0.10	0.20
0.05% Resistors (bridge)	4	4.20	16.80
AD4170-4 ADC (÷8)	1/8	29.33	3.67
STM32F0 (÷8)	1/8	0.31	0.31
Power Distribution (÷8)	1/8	4.10	0.51
PCB Manufacturing and Assembly (÷8)	1/8	10.00	1.25
Total (per channel)			**38.22**

The next solution analyzed was the instrumentation amplifier and Sallen-Key based circuit. The circuit schematic for this design is shown in Figrue 11.

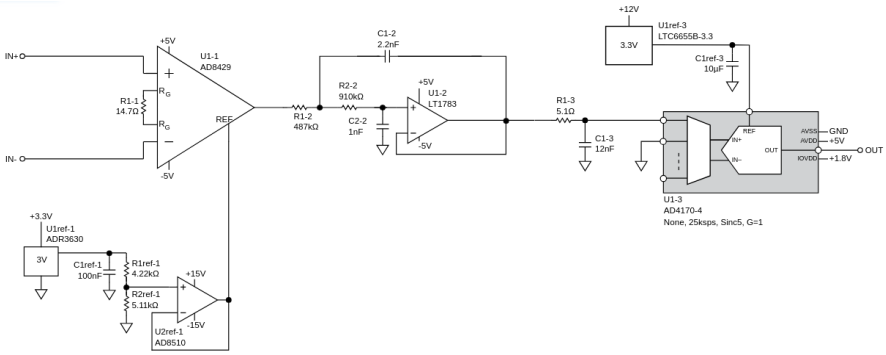

Figure 11: In Amp + Sallen-Key

As with the previous two circuits, noise simulation was performed and is presented in Figure 12. In this case, the sensor noise dominates and the total integrated noise falls to

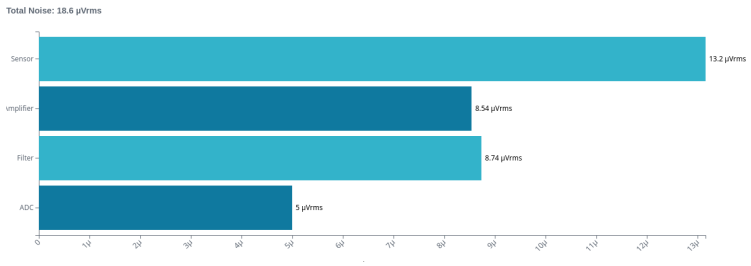

Figure 12: In Amp + Sallen-Key Total Noise

18.6 μVrms referred to the ADC input, roughly an order of magnitude below the 158 μVrms of the equivalent differential amplifier design. The error budget for this circuit is shown in Table 10.

Table 10: Error Budget: In Amp + SK

Category	**Offset**	**Rel. Error**
Total		
Total Error	186mV μV	0.697%
ADC		
Zero Error	80 μV	–
Gain Error	–	250 ppm
INL	–	2.5 ppm
Amplifier		
Offset	62.4 mV	–
Offset Current	2.15 mV	–
Gain Error	–	0.15%
CMRR	99.3μV	–
Resistors		
R1 Tol.	19.9 μV	0.494%
Filter Op Amp		
Offset	800 μV	–
Bias Current	112 mV	–
Offset Current	12.2 pV	–
CMRR	–	31.6 ppm
Filter Resistors		
R1 Tolerance	–	–
R2 Tolerance	–	–

The costs of the Instrumentation Amplifier and Sallen-Key filter circuit were analyzed and are presented in Table 11.

Table 11: Cost Budget: In Amp + Sallen-Key

Component	**Qty**	**Unit $**	**Total $**
AD8429 Amplifier (amp stage)	1	17.59	17.59
LT1783 Amplifier (filter stage)	1	5.56	5.56
0.5% Resistors	6	0.10	0.60
0.5% Capacitors	2	0.10	0.20
0.05% Resistors (bridge)	4	4.20	16.80
AD4170-4 ADC (÷8)	1/8	29.33	3.67
STM32F0 (÷8)	1/8	2.50	0.31
Power Distribution (÷8)	1/8	4.10	0.51
PCB Manufacturing and Assembly (÷8)	1/8	10.00	1.25
Total			**46.49**

The last circuit analyzed was the instrumentation amplifier and RC filter. The schematic for this circuit is shown in Figure 13.

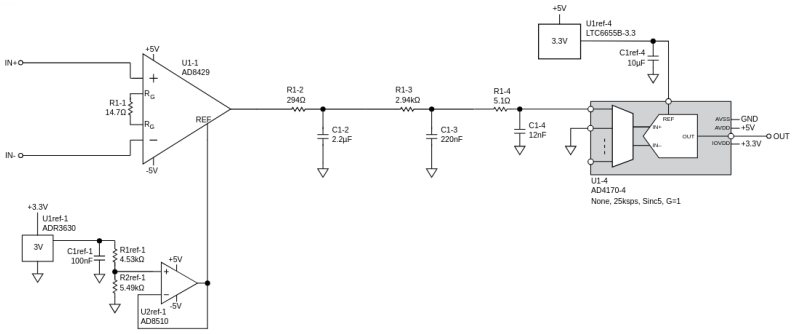

Figure 13: In Amp + RC Filter Circuit

The noise totals resulting from the Signal Chain Analyzer noise simulation are shown in Figure 14.

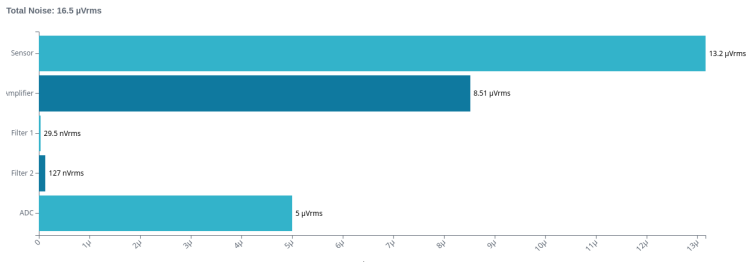

Figure 14: In Amp + RC Filter Total Noise

This solution showed slight improvement in noise performance over the Sallen-Key based implementation due to the removal of the op-amp in the filter stage, with a total integrated noise of 16.5 μVrms referred to the ADC input compared to 18.6 μVrms for the Sallen-Key variant. This is the lowest noise total of the four candidates. The error budget for this solution is shown in Table 12.

Table 12: Error Budget: In Amp + RC

Category	**Offset**	**Rel. Error**
Total		
Total Error	73.3 mV	0.694%
ADC		
Zero Error	80 μV	–
Gain Error	–	250 ppm
Input Current	130 μ V	–
INL	–	2.5 ppm
Amplifier		
Offset	62.4 mV	–
Offset Current	2.15mV	–
Gain Error	–	0.15%
CMRR	243nV	–
Resistors		
R1 Tol.	–	0.494 %
Filter Resistors		
R1 Tol.	–	–
R2 Tol.	–	–

Finally, the costs of the instrumentation amplifier and RC filter based solution were computed and are presented in Table 13.

Table 13: Cost Budget: In Amp + Sallen-Key

Component	**Qty**	**Unit $**	**Total $**
AD8429 Amplifier (amp stage)	1	17.59	17.59
0.5% Resistors	6	0.10	0.60
0.5% Capacitors	2	0.10	0.20
0.05% Resistors (bridge)	4	4.20	16.80
AD4170-4 ADC (÷8)	1/8	29.33	3.67
STM32F0 (÷8)	1/8	2.50	0.31
Power Distribution (÷8)	1/8	4.10	0.51
PCB Manufacturing and Assembly (÷8)	1/8	10.00	1.25
Total			**40.93**

This design achieved the lowest total noise and contibutes the lowest error to the signal chain. The cost falls between the figures for the instrumentation amplifier and Sallen-Key based circuit and the differential amplifier and Sallen-Key based circuit.

2.3 Solution Selection

The solutions were evaluated using the weighted objectives chart presented in the methodolgy section. The completed chart is presented in Table 14.

Table 14: Weighted objectives matrix.

Criterion	**Weight (%)**	**Diff+RC**	**Diff+SK**	**In+SK**	**In+RC**
Noise performance	50	2	2	8	8
Cost	30	10	6	1	3
Offset Error performance	10	8	4	4	8
Gain Error performance	10	4	4	8	8
Total	100	520	360	550	650

Based on the weighted objectives chart, the recommended solution is a signal conditioning system based on the instrumentation amplifier and 2nd order RC filter. This circuit performed the best in both the noise and error performance metrics. It costs $8 per input more than the cheapest design (Diff amp + RC) which is deemed to be sufficiently low to make it a worthwhile upgrade.

3 Conclusions

This report conducted a comparative analysis of design alternatives for a strain gauge signal conditioning system. The goal of this report was to produce a cost-effective solution that could be used to reduce the cost of performing strain measurements in academia. The report considered a two stage system consisting of an amplifier stage followed by a filter stage. Two alternatives consisting of the difference amplifier and the instrumentation amplifier were

considered for the amplifier stage. For the filter stage, both a 2nd order RC filter as well as a Sallen-Key filter were considered as design alternatives for a low pass filter.

Hand calculations were performed to determine component ratings for each circuit. The hand calculations were based on the engineering analysis inputs stated in Table 1. The amplifiers were designed for a gain of 412 V/V and the filters were designed for a cutoff frequency of 160Hz. The circuits were simulatd in Signal Chain Analyzer to determine their noise and error performance. All noise quantities were evaluated reffered to the ADC input. The error simulations considered gain and offset error sources from the amplifier, filter and ADC. Error simulation was conducted at 25^oC to eliminate drift error contributions from the simulated totals. The simulations showed that the use of an instrumentation amplifier significantly reduces the noise contribution of the amplifier stage. It is designed for high input impedance whereas the difference amplifier requires large gain setting resistors which increase Johnson noise contributions. The 2nd order RC filter outperformed the Sallen-Key filter in cost, error, and noise performance. After performing the simulations, each design was ranked using the weighted objectives chart presented in Table 14. Noise and cost performance were ranked the highest as error can be improved through calibration. The combination of an instrumentation amplifier and RC filter was deemed to be the optimal design configuration.

4 Recommendations and Future Work

Precision analog design is extremely complex. The findings of this report, while serving as a starting point, offer numerous areas for continued work. Practical circuits contain multiple additional noise sources that were neglected from the noise analysis in this report. A more robust analysis would consider the impact of noise sources like shot noise, burst noise, and 1/f noise. Additionally, circuits are operated in varying conditions which adds a drift contribution to the error analysis. Future work may consider the impact of drift on the offset and relative error totals. Furthermore, the results of this report are theoretical and a practical implementation is required to validate the results experimentally. It is the author's intent to design and manufacture a PCB after which experimental analysis using tools such as a spectrum analyzer may be performed to validate the noise and error totals.Future implementations may consider transistor-level amplifier design or the use of higher order filters to improve the performance of the system.

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A Appendix A: Circuit Design Hand Calculations

A.1 Amplifiers

A.1.1 Level Shift

Horrowitz and Hill chapter 5 section 12 describes the selection of level shift. Level shifting the input signal is required because the ADC cannot measure voltage below $0V$. Level shifting ensures the signal range $0mV \rightarrow -4mV$ remains in the ADC's operational range. The level shift should shift a signal of $0V$ to $\frac{V_{ref}}{2}$. This leads to $V_{shift} = 1.65V$. The level shift is realized by biasing the non inverting input of the respective amplifier by the amount specified by V_{shift} [8].

A.1.2 Gain

Horrowitz and Hill further describe the selection of amplifier gain in measurement circuits. The ideal gain is given by equation 10[4].

$$G = \frac{V_{ref} - V}{V_{sig}} \tag{10}$$

This equation arises from the the fact that maximal ADC resolution is obtained when V_{sig} is maximized under the constraint that V_{sig} must not exceed V_{ref}. This leads to $V_{sig} = V_{ref}$ as the optimal condition. The gain is set to achieve this. Inserting the values of V_{sig} and V_{ref} from Table 1 gives $G = 412$.

A.1.3 Instrumentation Amplifier

As discussed in Alexander and Sadiku, the gain of the instrumentation amplifier is determined by equation 7 introduced earlier, repeated below for convenience [8].

$$1 + \frac{2R}{R_G}$$

For the instrumentation amplifier selected for analysis (AD8429), the value of R obtained from the datasheet is $3k\Omega$ [9]. This yields $R_G = 14.7\Omega$. The rule of thumb for cascaded analog design is that the input impedance of a given stage should be a minimum of 10x the output impedance of the previous stage [5]. Because an integrated instrumentation amplifier is used, the input impedance is a datasheet parameter. For the AD8429 $R_{in} = 220G\Omega >> 10R_s$ [9].

A.1.4 Difference Amplifier

The difference amplifier equation relating the output voltage to the input is equation 6 introduced earlier, repeated below for convenience.

$$v_o = \frac{R_2(1 + \frac{R_1}{R_2})}{R_1(1 + \frac{R_3}{R_4})} v_2 - \frac{R_2}{R_1} v_1$$

Setting $\frac{R_3}{R_4} = \frac{R_1}{R_2}$ we can write the relationship as $v_o = G(v_2 - v_1)$ with $G = \frac{R_2}{R_1}$ which is a gain applied to a differential signal as desired. The differential amplifier has input impedance given by equation 11.

$$R_{in} = R_1 \tag{11}$$

Choosing $R_1 = 7.12k\Omega$ (satisfying $R_{in} > 10R_s$) results in $R_2 = 7.15M\Omega$. For the comparative analysis, the ADA4098 will be used for the differential amplifier's op-amp. The parameters are obtained from the ADA4098 datasheet provided by Analog Devices [10].

A.2 Filters

A.2.1 2nd Order RC Lowpass Filter

Su gives the frequency response of the first order RC filter as equation 8 introduced earlier, repeated below for convenience [7].

$$H(\omega) = \frac{1}{1 + j\omega RC}$$

According to the method of 2nd order RC filter design described by Su, a second order filter is achieved by adding a second RC network with the same cutoff frequency in cascade [7]. This method neglects the loading effect of the second stage with the first. Additionally, the cutoff frequency is calculated at $-6dB$ not $-3dB$ as is standard. The factor $\sqrt{\sqrt{2} - 1}$ must be applied to obtain the -3_{dB}. The value calculated below is the $-6dB$ cutoff that must be used so that the $-3dB$ point is at 160Hz. The filter components for the second stage are scaled so that the 10x rule of thumb is followed and the loading effect assumption is valid [8].

$$f_c = BW_{sig} \div \sqrt{\sqrt{2} - 1} = (160Hz)(1.554) = 249Hz \tag{12}$$

choosing $R_1 = 294\Omega$ gives $C_1 = 2.2\mu F$, $R_2 = 2940\Omega$ and $C_2 = 0.22\mu F$.

A.2.2 Sallen-Key Filter

The Sallen-Key filter is designed to implement a Butterworth filter with maximally flat passband frequency response. This filter consists of an op-amp, two resistors, and two capacitors. The op-amp gain should be set to $A_v = 1$. Choosing $R_f = R_i = 0$. If we choose equal values of resistors and capacitors, the cutoff frequency is $f_c = \frac{1}{2\pi RC}$. The addition of the op-amp has eliminated the loading effect. Since this is the same expression as the second order RC filter, we choose the same component values. For the comparative analysis, the LT1783 will be used as the Sallen-Key filter's operational amplifier its parameters were obtained from the datasheet provided by Analog Devices [11].

B Appendix B: Signal Chain Analyzer Noise and Error Analysis Outputs By Stage

The noise and error totals quoted in Section 2.2 are the aggregate of the individual stage contributions computed by Analog Devices Signal Chain Analyzer. This appendix reproduces

the per-stage outputs for each of the four building blocks used to assemble the candidate solutions, so that the origin of each total can be traced. For every stage the noise breakdown is given first, followed by the error budget. Noise contributions are quoted as rms values integrated to half the ADC sampling rate; error contributions are separated into an offset column and a gain column, and all figures are taken at 25 °C.

B.1 Differential Amplifier Stage

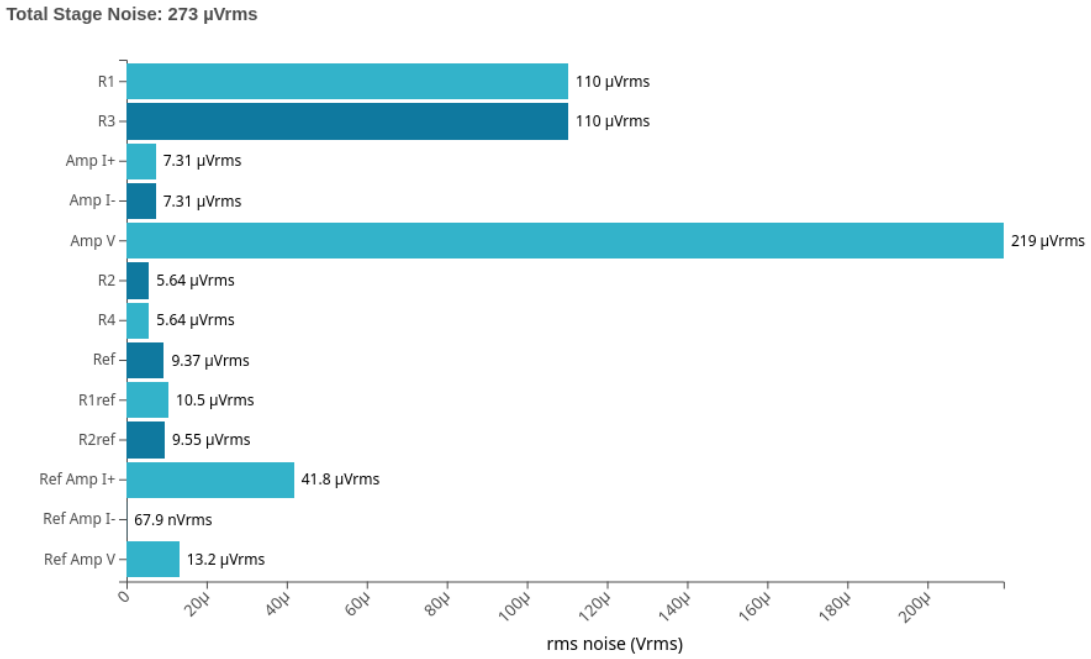

Figure 15: Differential amplifier stage noise breakdown. Total stage noise 273 μVrms, dominated by the amplifier voltage noise (219 μVrms) and the Johnson noise of the two 7.12 kΩ input resistors R1 and R3 (110 μVrms each).

Group/Id	Error Source	Spec Value	Sensitivity	Offset Error	Gain Error
Total Error				55.4µV	0.691 %
⌄ Op Amp					
	Offset	35µV	1	35.1µV	
	Offset Drift	500nV/°C	5.01	2.51µV	
	Bias Current	700pA	0		
	Bias Current Drift	121pA/°C	0		
	Offset Current	700pA	5.04k	3.53µV	
	Offset Current Drift	60.6pA/°C	25.2k	1.53µV	
	CMRR	120dB	499m		499 ppb
⌄ Ref					
	Initial Accuracy	400 ppm	4.14m	1.66µV	
	Drift	3 ppm/°C	20.7m	62.2nV	
	Load Regulation	15 ppm/mA	6.19µ	92.8pV	
⌄ Ref Amp					
	Offset	400µV	2.52m	1.01µV	
	Offset Drift	5µV/°C	12.6m	63.1nV	
	Bias Current	80pA	1.26k	100nV	
	Bias Current Drift	833fA/°C	6.28k	5.23nV	

Figure 16: Differential amplifier stage error budget. Total stage error 55.4 μV offset and 0.691% gain error.

B.2 Instrumentation Amplifier Stage

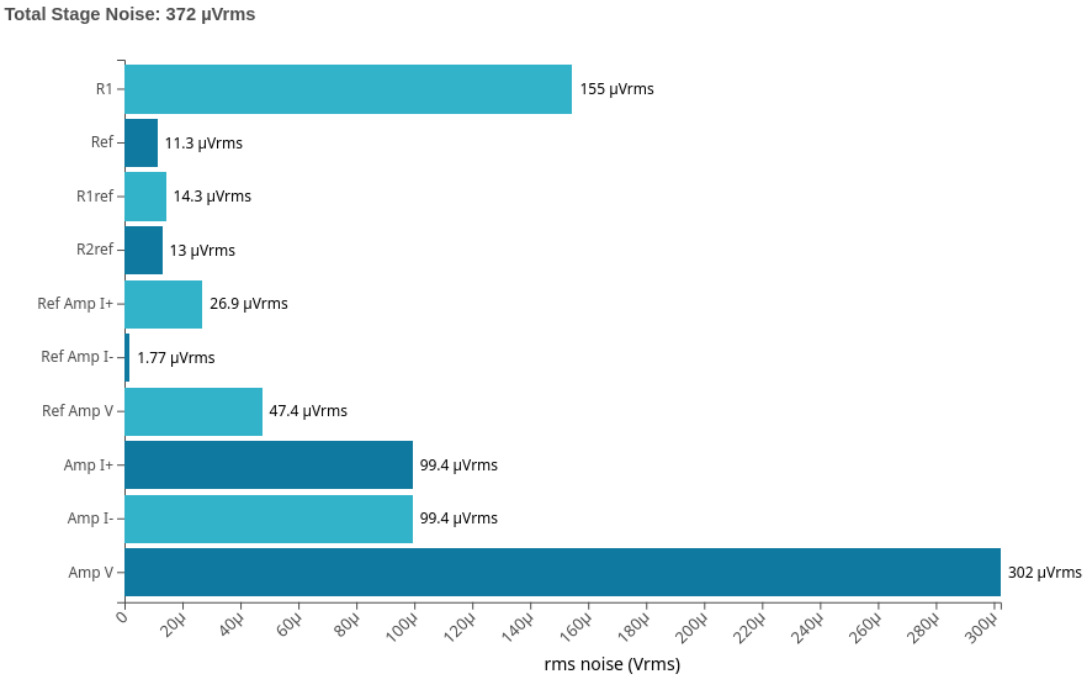

Figure 17: Instrumentation amplifier stage noise breakdown. Total stage noise 372 μVrms, dominated by the AD8429 voltage noise (302 μVrms) and its input current noise (99.4 μVrms on each input).

Group/Id	Error Source	Spec Value	Sensitivity	Offset Error	Gain Error
Total Error				62.6mV	0.516 %
⌄ In Amp					
	Offset	152µV	409	62.4mV	
	Offset Drift	1.02µV/°C	0		
	Bias Current	150nA	0		
	Bias Current Drift	250pA/°C	0		
	Offset Current	30nA	71.6k	2.15mV	
	Offset Current Drift	500pA/°C	0		
	Gain Error	0.15 %	1		0.15 %
	Gain Drift	99.8 ppm/°C	0		
	CMRR	132dB	409	99.3µV	
⌄ Ref					
	Initial Accuracy	400 ppm	1.64	657µV	
	Drift	3 ppm/°C	0		
	Load Regulation	15 ppm/mA	528m	7.92µV	
⌄ Ref Amp					
	Offset	400µV	1	400µV	
	Offset Drift	5µV/°C	0		

Figure 18: Instrumentation amplifier stage error budget (part 1 of 2). Total stage error 62.6 mV offset and 0.516% gain error; the offset is dominated by the 152 μV input offset voltage acting through the stage gain of 409.

Group/Id	Error Source	Spec Value	Sensitivity	Offset Error	Gain Error
	Drift	3 ppm/°C	0		
	Load Regulation	15 ppm/mA	528m	7.92µV	
Ref Amp					
	Offset	400µV	1	400µV	
	Offset Drift	5µV/°C	0		
	Bias Current	80pA	2.31k	185nV	
	Bias Current Drift	N/A	0	NaNV	NaN
	Offset Current	75pA	49.1m	3.68pV	
	Offset Current Drift	N/A	0	NaNV	NaN
	CMRR	86dB	0		
Resistors					
	R1 Tolerance	0.5 %	988m		0.494 %
	R1 Drift	25 ppm/°C	0		
	R1ref Tolerance	0.5 %	740m	3.7mV	
	R1ref Drift	25 ppm/°C	0		
	R2ref Tolerance	0.5 %	739m	3.7mV	
	R2ref Drift	25 ppm/°C	0		

Figure 19: Instrumentation amplifier stage error budget (part 2 of 2), showing the reference amplifier and resistor tolerance contributions. The 0.5% gain resistor R1 accounts for 0.494% of the 0.516% total gain error.

B.3 Second Order RC Filter Stage

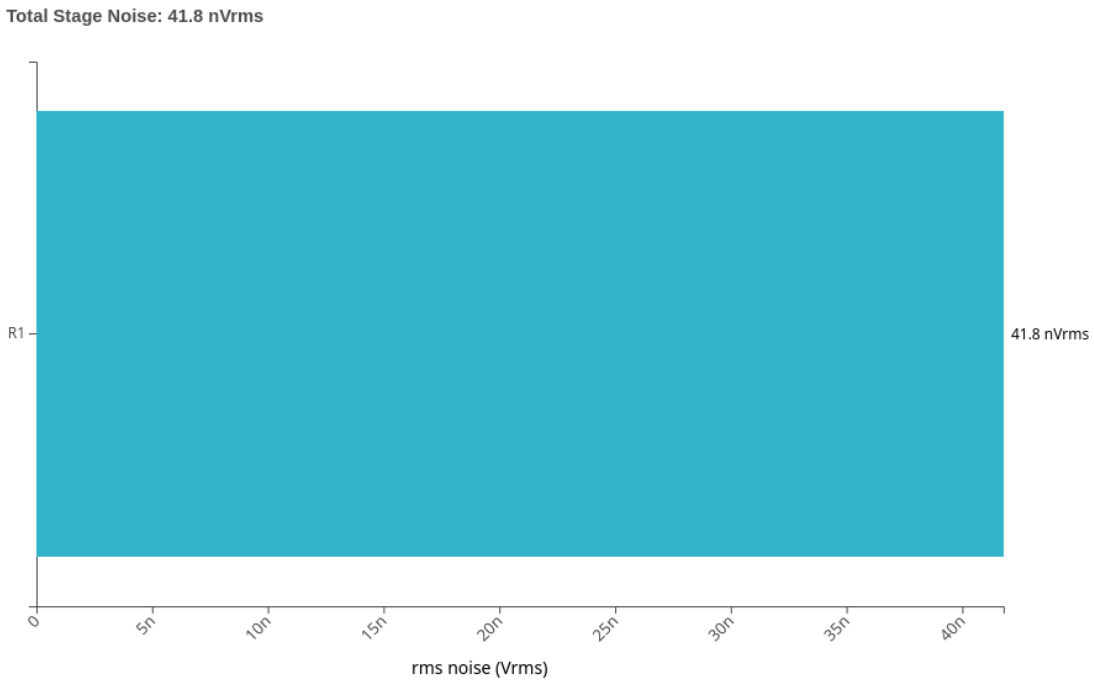

Figure 20: Second order passive RC filter stage noise breakdown. Total stage noise 41.8 nVrms, arising solely from the Johnson noise of the filter resistors; the passive filter contributes roughly four orders of magnitude less noise than either amplifier stage.

Group/Id	Error Source	Spec Value	Sensitivity	Offset Error	Gain Error
Total Error				0V	0
⌄ Resistors					
	R1 Tolerance	0.5 %	0		
	R1 Drift	25 ppm/°C	0		

Figure 21: Second order passive RC filter stage error budget. The stage contributes no offset error and no gain error, because the DC gain of the filter is independent of the resistor values and the network is entirely passive.

B.4 Sallen-Key Filter Stage

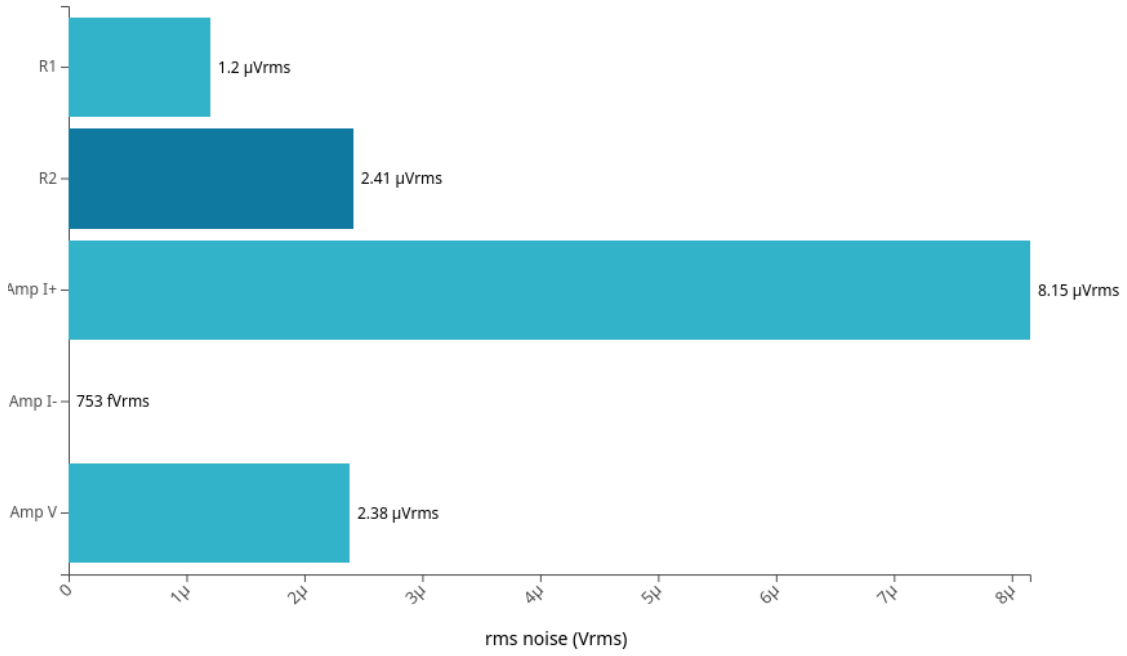

Figure 22: Sallen-Key filter stage noise breakdown. The LT1783 input current noise (8.15 μVrms) and voltage noise (2.38 μVrms) dominate. The active filter contributes more noise than the passive RC network of Figure 20.

Group/Id	Error Source	Spec Value	Sensitivity	Offset Error	Gain Error
Total Error				112mV	31.6 ppm
Op Amp					
	Offset	800µV	1	800µV	
	Offset Drift	5µV/°C	0		
	Bias Current	80nA	1.4M	112mV	
	Bias Current Drift	60pA/°C	0		
	Offset Current	8nA	1.52m	12.2pV	
	Offset Current Drift	97pA/°C	0		
	CMRR	90dB	1		31.6 ppm
Resistors					
	R1 Tolerance	0.5 %	0		
	R1 Drift	25 ppm/°C	0		
	R2 Tolerance	0.5 %	0		
	R2 Drift	25 ppm/°C	0		

Figure 23: Sallen-Key filter stage error budget. Total stage error 112 mV offset and 31.6 ppm gain error. The offset is dominated almost entirely by the 80 nA op-amp bias current acting through the 1.4 MΩ sensitivity of the filter network.

C Appendix C: Datasheet Excerpts

The rms noise figure used for the AD4170-4 throughout this report is a typical datasheet parameter rather than a calculated quantity. Figure 24 reproduces the relevant section of the AD4170-4 data sheet, which states the methodology used to obtain it: the values are generated by gathering 1000 samples at a differential input voltage of 0 V with the converter continuously converting on a single channel, using the bipolar input range and an external 2.5 V reference [12]. The excerpt also gives the definition of effective resolution used in equation 4, and Table 6 of the data sheet lists the rms noise against output data rate and gain setting.

RMS NOISE AND RESOLUTION

Table 6 through Table 17 show the RMS noise, peak-to-peak noise, effective resolution, and noise-free (peak-to-peak) resolution of the AD4170-4 for various ODRs, gain settings, and filters. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated by gathering 1000 samples with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the effective resolution is calculated using the RMS noise, whereas the peak-to-peak resolution (shown in parentheses) is calculated based on peak-to-peak noise (shown in parentheses). The peak-to-peak resolution represents the resolution for which there is no code flicker.

$$\textit{Effective Resolution} = \text{Log}_2(\textit{Input Range}/\textit{RMS Noise}) \quad (1)$$

$$\textit{Peak-to-Peak Resolution} = \text{Log}_2(\textit{Input Range}/\textit{Peak-to-Peak Noise} \quad (2)$$

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Table 6. RMS Noise (Peak-to-Peak Noise) vs. Gain and ODR (µV)

Filter Word (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 0.5	Gain = 1 Precharge	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
65,532	7.63	3.38	0.28 (1.2)	0.14 (0.59)	0.13 (0.6)	0.076 (0.45)	0.043 (0.24)	0.033 (0.22)	0.025 (0.15)	0.018 (0.12)	0.014 (0.093)	0.013 (0.084)
50,000	10	4.43	0.26 (1.2)	0.14 (0.59)	0.14 (0.6)	0.076 (0.45)	0.048 (0.24)	0.038 (0.22)	0.029 (0.19)	0.02 (0.13)	0.016 (0.093)	0.014 (0.084)
25,000	20	8.85	0.33 (1.8)	0.16 (0.89)	0.18 (1.19)	0.10 (0.6)	0.066 (0.37)	0.05 (0.3)	0.041 (0.27)	0.027 (0.17)	0.023 (0.14)	0.019 (0.12)
10,000	50	22.13	0.49 (3.6)	0.21 (1.19)	0.25 (1.49)	0.16 (1)	0.10 (0.67)	0.078 (0.52)	0.068 (0.4)	0.043 (0.25)	0.036 (0.2)	0.03 (0.18)
8,332	60	26.59	0.53 (3.6)	0.22 (1.19)	0.26 (1.49)	0.16 (1.1)	0.11 (0.68)	0.087 (0.63)	0.069 (0.41)	0.047 (0.3)	0.039 (0.24)	0.034 (0.19)
5,000	100	44.25	0.66 (4.2)	0.3 (2.1)	0.35 (2.1)	0.21 (1.34)	0.14 (0.89)	0.12 (0.78)	0.092 (0.58)	0.062 (0.4)	0.048 (0.35)	0.042 (0.24)
1,000	500	221.25	1.4 (8.3)	0.6 (3.8)	0.75 (4.8)	0.45 (2.7)	0.31 (2)	0.25 (1.6)	0.2 (1.3)	0.14 (0.9)	0.11 (0.74)	0.092 (0.6)
500	1,000	442.5	2.1 (12.5)	0.9 (6)	1 (6.3)	0.63 (3.9)	0.44 (3)	0.36 (2.6)	0.28 (1.5)	0.2 (1.4)	0.16 (0.96)	0.13 (0.75)
100	5,000	2,206	4.5 (29.8)	1.9 (11.9)	2.4 (15.5)	1.4 (8.6)	0.94 (6)	0.8 (5.4)	0.64 (3.7)	0.44 (3)	0.36 (2.4)	0.3 (1.8)
80	6,250	2,758	5 (31)	2.2 (13.4)	2.6 (16.7)	1.5 (10.1)	1.1 (7.9)	0.9 (6.1)	0.7 (4.4)	0.5 (3.2)	0.4 (2.7)	0.33 (2)
48	10,416.7	4,565	6.5 (42.3)	2.7 (18.2)	3.3 (21.2)	2 (12.8)	1.4 (8.6)	1.1 (7.1)	0.9 (6.2)	0.63 (4.1)	0.5 (3.3)	0.43 (3.2)
40	12,500	5,455	7 (47.1)	2.9 (19.7)	3.7 (22.9)	2.2 (13.7)	1.5 (9.8)	1.3 (7.6)	1 (6.3)	0.68 (4.5)	0.55 (3.5)	0.47 (3.5)
20	25,000	10,483	9 (57.2)	4.2 (26.2)	5.1 (34.3)	3.1 (20.9)	2.2 (13.2)	1.8 (10.1)	1.4 (8.8)	1 (6.7)	0.78 (5.2)	0.68 (4.4)
16	31,250	12,741	10.2 (64.3)	4.7 (30.4)	5.5 (35.2)	3.4 (22.9)	2.4 (16.3)	1.9 (12.6)	1.5 (10.2)	1.1 (7.6)	0.9 (6)	0.76 (5.2)
12	41,666.7	16,047	11.7 (70.3)	5.1 (35.2)	6.3 (39.6)	3.8 (24.9)	2.6 (17)	2.2 (13.1)	1.8 (11.3)	1.3 (7.7)	1 (6.5)	0.89 (5.7)
8	62,500	21,019	14.3 (90.6)	6.1 (47.1)	7.6 (47.1)	4.5 (28.2)	3.2 (18.6)	2.7 (17.1)	2.1 (13.1)	1.5 (9)	1.2 (8)	1.1 (7.3)
4	125,000	27,618	16.6 (100)	7.3 (41.4)	9 (55.4)	5.5 (34.3)	3.9 (26.8)	3.2 (19.8)	2.7 (17.8)	1.8 (11.4)	1.6 (11.1)	1.4 (9.7)

Figure 24: AD4170-4 data sheet excerpt describing the rms noise and resolution specification and its measurement methodology [12].